34053 – Very Large Scale Integration

1. Combinational Logic Circuit
Part – A
1. Draw the AND gate Circuit using CMOS?
2. What are races? What are its types?
3. Define Logic Network?
4. Define Critical races?
5. Define SOP & POS?
6. What do you mean by Hazards in Digital Circuits?
7. Define Glitch in Digital Circuits?
8. Draw the CMOS OR Gate Circuit?
9. Why CMOS is better than NMOS & PMOS in realization of gates?
10. Distinguish between encoder & decoder?

Part – B
1. Draw the circuit of Half adder & explain with truth table?
2. Explain CMOS Inverter gate?
3. What is Mux? Draw the graphical symbol & truth table of 4X1 Mux?
4. What are Hazards? How do eliminate them in digital Circuits?
5. Explain about the Encoder Circuit?

Part – C
1. Explain the CMOS AND, OR, inverter and explain with truth table?
2. Implement the function F={1,2,3,5,7,10,13} with minimal gates?
3. What is decoder? Implement the full adder using a decoder?
4. Implement f=∑m(1,3,5,8,9,11,15)+d(2,13) with Minimal gates? & implement the same function using a Mux?
5. Draw & explain the CMOS AND, OR & NAND gate?
6. i) Implement the Function F=∑m(1,2,3,5,7,10,13) with minimal gates?
   ii) Implement the Function F=∑m(0,2,3,7) with mux?

2. VHDL for Combinational Circuits
Part - A
1. Define the Simulation?
2. Expand & Define VHDL?
3. List any two assignment statement?
4. List ant two logical operators?
5. Define the term Synthesis?
6. Write the VHDL Code for OR gate?
7. What are the types of generating Statement?
8. Define Design entry?
9. Define relational operators?
10. State the VHDL Concurrent Signal assignment statements?
11. Write the VHDL Code for 2 input AND gate?

Part – B
1. Explain about logical operators?
2. Define Concurrent Signal Assignment?
3. Write the VHDL Code for NAND Gate?
4. Write the VHDL Code for AND & NOT Gate?
5. Write the syntax of Architecture?
6. Explain about the Architecture in VHDL?
7. Explain about the Arithmetic Operators?
8. Write the Syntax of Simple Signal assignment statement with an example?
9. What is process Statement? Give the syntax of the process Statement?

Part – C
1. Develop a VHDL Code for 3:8 Decoder & OR Gate?
2. Develop a VHDL Code for 4:2 Encoder & NAND Gate with truth table?
3. Write a VHDL Code for 1X2 Demultiplexer. Draw the truth table & the Logic diagram of 1X2 Demultiplexer?

4. Explain in detail about the Assignment statements?
5. Write the VHDL code for 8:3 encoder?
6. Write a VHDL Code for 2X1 Multiplexer. Draw the truth table & the Logic diagram of 2X1 Multiplexer?
7. Develop a VHDL Code for 2X4 Decoder & explain with truth table?
8. Explain in detail about the VHDL operators?
9. Develop a VHDL Code for 4:1 & 8:1 Multiplexer?

3. Sequential Logic circuits
Part – A

1. What are the types of Shift Register?
2. Write the excitation table of JK FF?
3. Define Storage elements?
4. Define State table?
5. Write the importance of JK and T Flip flop?
6. Are Latch and Flip flop are same?
7. What is Mealy & Moore Machine?
8. Expand and define SIPO, PIPO?

Part – B

1. Write down the count sequence for Modulo 8 Counter?
2. What is an Excitation table & Write the excitation table for D-FF?
3. Distinguish between Mealy & Moore machine?
4. What are the steps involved in designing a synchronous Sequential Circuit?
5. Distinguish between a Latch & Flip flop?
6. Define State Diagram & State table?
7. Write the Excitation table for D & T FF?

Part – C

1. Design a Modulo 8 Counter using DFF. Use a Proper Excitation table & State Diagram?
2. Design a Modulo 6 Counter using DFF. Use a Proper Excitation table & State Diagram?
3. Design a Modulo 5 Counter using DFF. Use a Proper Excitation table & State Diagram?
4. Design a Modulo 7 Counter using DFF. Use a Proper Excitation table & State Diagram?
5. Design a Modulo 4 Counter using DFF. Use a Proper Excitation table & State Diagram?

4. VHDL for Sequential Circuit
Part – A

1. Write the VHDL Code for entity body of decade counter?
2. Write the importance of D Latch?

Part – B

1. Write a VHDL Code for D Latch?

Part – C

1. Write a VHDL Code for JK FF with reset input?
2. Write a VHDL Code for Decade Counter?
3. Write a VHDL Code for JK FF without reset input?
4. Write a VHDL Code for Johnson Counter?
5. Write an VHDL Code for T FF with reset input?
6. Write an VHDL Code for 2 Bit up Counter?

5. PLDs and FPGA
Part – A

1. Define PAL?
2. Expand CPLD?
3. What are the types of ASIC?
4. Expand PLA?
5. What are the demerits of PLA?
6. Compare PLA & PAL?
7. Define PROM?
8. Expand & define FPGA & CPLD?

34053 – Very Large Scale Integration

Part – B

1. Expand & Define FPGA?
2. What are the advantages of PLA?
3. Draw the Block Schematic of CPLD?
4. What are the types of ASIC?
5. Explain the features of Product term expansion in PAL?
6. Draw the Block Diagram of FPGA?

Part – C

1. Implement the Following function in PLA F=$\sum$ (1, 5, 7, 11.15)?
2. Implement the Following function F=$\sum$ (1, 2, 4, 6) in PAL?
3. Explain in detail about the FPGA?
4. Implement the Following function F=$\sum$ (0, 2, 6, 7, 8 , 9,12, 13,14) in PAL?
5. Explain in detail about the CPLD with its Block Diagram?
6. Explain in detail about the PAL & PLA?